Packaging Failure Isolation with Time-Domain Reflectometry (TDR) for Advanced BGA Packages

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Abstract
IC packages become increasingly complex, which make failure analysis (FA) very challenging. This paper presents advanced packaging failure isolation with time-domain reflectometry (TDR), where the efforts are put on comparative method investigation. Flip-chip ball grid array (fBGA) and stacked-die low-profile fine-pitch BGA (stacked-die LFBGA) packages are used to demonstrate advanced packaging FA isolation with TDR and good practices in analysis are highlighted, including signature quality improvement and ground selection. The paper also uses software to mimic and observe TDR signature under various failure modes in order to study TDR behavior with different failure modes. The acquired observations are helpful in packaging FA isolation with TDR.

1. Introduction

With the advance of semiconductor technology, more functions are integrated into single die and more dies are assembled into one package. Therefore, packages become increasingly complex with the growing size and I/O number, which raises great challenges on packaging failure analysis (FA) [1]. Traditional FA approaches using the equipments such as x-ray and scanning acoustic microscopy cannot fast and efficiently detect and isolate all the failures in the current developed packages due to its structural complexity like 3D packaging. Hence, although those approaches will continue playing great roles in packaging FA analysis for advanced packaging development, it is necessary to develop new approach to detect and isolate the failures, which those equipments fail to find out.

Time-domain reflectometry (TDR) is an instrument for time-domain electrical characterization [2]. TDR generates step signal with very sharp edge and injects this pulse into packaging interconnect. Through the reflected or transmitted signal detected by TDR, interconnect behavior including packaging failure inside packages is determined. Recently, TDR gains the great attention and becomes popular in packaging failure analysis and isolation due to its unique advantages[3-5]. The engineers have placed much effort on TDR to exploit and extend its FA analysis capability for various advanced packages, among which comparative method is dominant [6, 7]. This paper focuses on failure detection and isolation for flip-chip BGA package and stacked-die LFBGA package with comparative method.

2. TDR Fundamental

As a nondestructive technique, FA analysis with TDR uses the information derived from the reflected wave to determine where package fails. Fig. 1 shows how TDR operates in FA analysis. TDR first generates a step signal with very sharp edge, which typically has several ten pico-seconds rise time and covers the spectrum larger than 10 GHz. When it is injected into packaging interconnect, it propagates along signal path. Most parts of this path can be regarded as transmission lines with the controlled characteristic impedance. However, when the signal arrives somewhere the discontinuity occurs, part of its energy is reflected.

\[ V_{ref} = \frac{Z - Z_0}{Z + Z_0} V_{in} \]  

where \( V_{ref}, V_{in} \) is the reflected and incident voltage of the signal, and \( Z, Z_0 \) is the impedance seen by the signal at the discontinuity and characteristic impedance of the transmission line. When interconnect opens,

\[ z = \infty \quad \text{and} \quad V_{ref} = V_{in} \]  

and when interconnect shorts to ground,

\[ z = 0 \quad \text{and} \quad V_{ref} = -V_{in} \]  

Because TDR instrument detects the sum of incident and reflected signal, the signal acquired at open failure location is \( 2V_{in} \) while it is 0 at short failure location.

However the path in practical package is not perfect transmission line, which usually consists of transmission lines with approximate constant characteristic impedance and lots of small discontinuities such as via, solder ball, and bonding wire. Those discontinuities will cause reflection, which overlie with main reflection from failure location. Hence, failure signature is contaminated, which increases the difficulty on failure detection and isolation. Another challenge is TDR resolution, which determines how small structures TDR can be separated through TDR signal. Comparative method, a predominant approach in FA analysis with TDR, uses three units, that is, failing unit, golden unit, and substrate (or leadframe). After setting up measurement, probe opening, failing unit, golden unit, and substrate unit are measured one by one for the failing pin. Through comparing the acquired four signals, failure location is detected. It provides several advantages:

Provide reference signature;
Provide critical locations including the locations of probe tip and substrate (or leadframe) end.
Increase the resolution.

Because FA analysis with TDR uses impedance change along signal path to detect failure location, it is critical to find out where part or ball is used properly as return path through...
packaging design. Otherwise, the failure signature is indistinct.

3. FA Analysis for fcBGA Package

A fcBGA package shown in Fig. 2 is used in the paper, which has the size of 40mmx40mm and 1517 balls with 8-layer substrate. Through test, it is found that the net connecting to solder ball AT2 fails, but it is unknown where it fails. In order to isolate this failure location, Tektronix DSA8200 and 80E04 sampling module are used for FA isolation. Because multi-reflection will cause failure signature indistinct, IConnect is also applied to eliminate it in the acquired signals. The samples include golden unit, failing unit, and substrate, necessary for comparative FA analysis. First, ball AT2 referenced with ball AU1 is probed one by one for three samples, and the acquired original voltages are shown in Fig. 3.

![Fig. 2 fcBGA package used in FA analysis.](image)

Fig. 2 The original voltage waveforms measured by TDR between nets AT2 and AU1.

Fig. 4 shows the impedance derived from Fig. 3 after the elimination of multi-reflection with IConnect. From Fig. 4 and packaging design, it is clear that in very short time after the signal is injected into the package through solder ball and before it arrive the trace in the first layer, the signal encounters an open failure in its path. Definitely, this failure lies in via. Fig. 5 verifies it through X-section of the package, and it is found that via’s pad is missing in the net.

As mentioned in last section, return path is critical in failure isolation with TDR for clear failure signature, and proper return path can produce good quality failure signature. With this fcBGA package, other neighboring solder balls around net AT2 are selected respectively and used as return path to show how large impact return path has on failure signature. The acquired results are shown in Fig. 6-8, where nets AR1, AR3, and AU3 are selected respectively as return path. Compared those with Fig. 4, it is found that with different return paths, the totally different signals and failure signatures are acquired. Among them, the signature acquired with net AU1 as return path (Fig. 4) is the easiest to identify and isolate failure location while the one done with net AU3 as return path (Fig. 8) is the most difficult. For this, it is impossible to find where fails because the signals from failing unit, golden unit and substrate are very similar. Hence finding a proper return path in failure analysis with TDR is critical. However, how can we select proper return path? First of all, the solder ball of return path should be around the ball of the failing net. Not only large probing spacing is inconvenient for probing, but also it introduces large discontinuity with much reflection at the probe tip. Power or ground plane in package is the first choice for return path if they support most parts of the trace of the failing net. But it is not always true in practical situations. For example, might all planes are floated in test package vehicle and there is not any solder ball connected to them. As alternative, we look for its immediate neighboring net as return path. Among all the viable nets, we need select a net, of which most part is parallel routed with the failing net and they are close each
other. The closer they are, structural change around them has the smaller impact on failure signature, which make failure isolation easy. Fortunately with the semiconductor advance, the recent designed advanced packages normally work on high speed, in which the impedance of most traces is well controlled referenced with power/ground plane. Therefore, those packages are very suitable for FA analysis with TDR.

4. FA Analysis for Stacked-Die FLBGA Package

In stacked-die package, failure isolation presents the great challenge, especially in a fine-pitch low–profile stacked-die BGA package with die arrangement shown in Fig 9, where three stacked dies are arranged so that the largest die is at top and the smallest is at bottom. Fig. (a) shows its cross-section and (b) is bottom view of this package. Although this package has small size with small I/O number and has only two layers, the failure in the first-level interconnect is very difficult to find out with traditional approaches. In this test vehicle, there is interconnect between dies through bond fingers in the same

(a) Die stacking (b) Bottom view

Fig. 9  Die stacking and bottom view of stacked-die FLBGA package.

et, which places additional challenge on packaging FA isolation. According to the discussion provided in last section, we need consider proper return path not only for trace but also for wire bond in FA analysis of this package with TDR. With proper selection of return path for the failing net, failing unit, golden unit, and substrate are probed one by one, and the acquired impedance profiles are shown in Fig. 10. It is very clear from Fig. 10 that the failure occurs at wire bond side, and the second wire bond might have the problem in this failure mode. It is also found the trace in the package is very short and it is less than 100ps, however, wire bond is very long.

5. TDR Behavior of Failure Mode through Simulation

It is very difficult to explore all possible failure modes through measurement because the samples with proper failure modes are unavailable, however, which is critical to accurately and efficiently isolate the failure in FA analysis with TDR in the future as the failure can be successfully detected and isolated only after TDR phenomenon and signature behavior for all possible failure modes is well known. Fortunately, circuit simulator can give us the assistance to mimic all the scenarios and failure modes existing in the failing units. Fig. 11 shows circuit schematic used here, which

Fig. 10  The impedance profile extracted from time-domain voltages in the failing ball of FLBGA package.

represents a typical net in wirebond BGA package, cable, probe and pulse generator used in TDR measurement for failure isolation. In order to mimic open conditions at different locations, a resistor with 1Mohm is inserted into the

Fig. 12  TD voltage when opening failures are at solder ball, trace and wire bond, compared with reference waveform from golden unit, substrate, probe opening.

failure locations. Fig. 12 shows TDR signatures (time-domain voltage) when open failures occur at wirebond, trace, and solder ball respectively. Compared with those from
probe opening, substrate, and golden unit. Fig. 13 shows TDR signatures when shorting failures occur at wirebond, trace, and solder ball respectively, compared with those from probe opening, substrate, and golden unit, where a resistor with 1mohm is inserted between failure locations and ground to mimic shorting failures. Through Fig. 12 & 13, it is found that the signatures are different with different failure locations, and it is very convenient to detect and isolate where the failure occurs (solder ball, wirebond, or trace), and what

failure occurs (opening or shorting). For example, high impedance in wire bond opening occurs only later than in substrate sample although this interval is small. However, it is enough for comparative approach to separate them.

Normally FA isolation can only detect and isolate complete failure, that is, total opening or shorting. But sometime there are lots of situations, where opening or shorting is incomplete. What will happen in FA analysis with TDR if those situations occur? As electrical behavior of such scenarios can be emulated with equivalent interconnect resistance, circuit simulator is used here to mimic incomplete shorting and opening at the trace in a wirebond BGA package close to wirebond to characterize electrical behavior and TDR signature of those failures. Fig 14 and 15 show time-domain voltage waveforms for

Fig. 14  TD voltage caused by different opening failure conditions at trace near wire bond compared with reference waveform from golden unit and substrate.

trace opening and shorting respectively with different degree of failure in terms of resistance. It is found that the opening

failure with larger than 500hm contact resistance can be easily isolated while the shorting failure with smaller than 100ohms contact resistance can be easily detected.

6. Conclusions

The paper presents advanced packaging failure analysis with time-domain reflectometry (TDR), and explores FA analysis of fBGA and stacked-die FLBGA packages in order to isolate failure types and locations. The emphases are placed on comparative method investigation, failure signature quality, and the impact of return path. With proper return path, failure signature can be improved, which is highlighted in the paper. The efforts are also put on the exploration of different failure modes and their signatures with circuit simulator, including incomplete opening/shorting failure. It is a good way through which various signatures with different failures are acknowledged for future FA isolation.

As a complementary approach, TDR is a good tool for packaging failure isolation. It is especially suitable for FA isolation of high-speed package as the impedance of signal traces in those packages is well controlled. The acquired insights in the paper can guideline practical FA analysis with TDR in the future.

References


